

Exhibit 4C

RCS file: /s6/cvsroot/euterpe/BOM,v

Working file: BOM

head: 5.105

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 1940; selected revisions: 11

description:

top level BOM

revision 4.0

date: 1995/08/10 08:26:48; author: chip; state: Exp; lines: +1 -1

Release Target: euterpe

The id chip is being used by tbr.

top level.0 prior to major build, 2nd attempt

revision 3.954

date: 1995/08/10 08:26:36; author: chip; state: Exp; lines: +4 -4

releasebom: File needs to be up-to-date to use commit -r

revision 3.953

date: 1995/08/10 05:54:16; author: chip; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc

analog_euterpe.hwc

The id chip is being used by tbr.

put vddep0/1 back to 20.5

revision 3.952

date: 1995/08/10 05:39:13; author: chip; state: Exp; lines: +2 -2

Release Target: euterpe/doc

The id chip is being used by tbr.

releasing to get included in full top level release

revision 3.951

date: 1995/08/10 00:01:32; author: mws; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc

cc/cc.V cc/cc_control_blob.pim:

CPlastIfetchI2 was not tau aligned and therefore could trigger cc/inprogpl to release the same cycle as a valid dmissR12. This can result in ccstartR13 the next cycle which is too fast for aSel to get the correct addresses loaded.

This was noticed by cachesynchnasty2_var_b_1 after the nb leak chck was added.

euterpe.V cp/cp.V cp/cphh.pim \

ce/cerberus.V ce/ce_mck.V ce/cerberus.cpf ce/cerbttest.V ce/cerbnobreg.V:

Synchronizer for machine check edge detector.

chip_euterpe-base.pim:

Added synchronizer placements in cp area.

uu/uu.V: Comment that swapstore load pipe only def on load1st was incorrect.

uu/uustepuu.pla: Because swapstore's step0 can issue on non-eta3, address generation must be a care. Add comments explaining barely-working performance-hurting mess of swpBsy, swpStr, and swpLd if step0 plays on eta2 or (worse) eta0.

revision 3.950
date: 1995/08/09 04:59:53; author: chip; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/lvs

The id chip is being used by tbr.
adding Hermes device

revision 3.949
date: 1995/08/09 04:46:39; author: chip; state: Exp; lines: +2 -2
Release Target: euterpe/verilog
Makefile

The id chip is being used by tbr.
Makefile no longer redirects outputs

revision 3.948
date: 1995/08/09 04:41:15; author: chip; state: Exp; lines: +2 -2
Release Target: euterpe/compass/layouts

The id chip is being used by tbr.
releasing latest frame cell edits

revision 3.947
date: 1995/08/09 04:29:54; author: chip; state: Exp; lines: +3 -3
Release Target: euterpe
.checkoutrc
Makefile

The id chip is being used by tbr.
tweak for top level build

revision 3.946
date: 1995/08/08 18:06:48; author: mws; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc

Checkins mostly to be compatible with new more rigorous VEqn var reuse checking.
at/atpadcd.Veqn nb/nbwe.Veqn:

Was dangerously using same symbol as vector & scalar I/O (but did work OK).
hc/hc_tagmatch.V:

Delete unnecess include of hc.h, for which Makefile did not enforce dependency.

uu/sswap.tst: Specify dlva to stop align check going X.

tst/drvchk.V: Update to match new single ended CEprb[31:0].

Some ICC and CC wires were floating in mgnb testing.

tst/vervars tst/tstgen: Were referencing non-stable non-std version of perl.

revision 3.945
date: 1995/08/05 15:18:55; author: chip; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc
chip_euterpe-base.pim

The id chip is being used by tbr.
move 2 components in nb

=====

RCS file: /s6/cvsroot/euterpe/compass/BOM,v
Working file: compass/BOM

head: 7.21
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 67; selected revisions: 2
description:

revision 6.0
date: 1995/08/10 05:42:46; author: chip; state: Exp; lines: +1 -1
Release Target: euterpe

The id chip is being used by tbr.
full release prior to major baseplate rebuild

revision 5.1
date: 1995/08/09 04:40:59; author: chip; state: Exp; lines: +2 -2
Release Target: euterpe/compass/layouts

The id chip is being used by tbr.
releasing latest frame cell edits
=====

RCS file: /s6/cvsroot/euterpe/compass/layouts/BOM,v
Working file: compass/layouts/BOM
head: 27.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 79; selected revisions: 2
description:
releasebom adding BOM

revision 20.0
date: 1995/08/09 04:40:50; author: chip; state: Exp; lines: +1 -1
Release Target: euterpe/compass/layouts

The id chip is being used by tbr.
releasing latest frame cell edits

revision 19.1
date: 1995/08/09 04:40:43; author: chip; state: Exp; lines: +16 -7
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/compass/layouts/euterpelpadtl.ly,v
Working file: compass/layouts/euterpelpadtl.ly
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3; selected revisions: 1
description:

revision 2.3

date: 1995/08/07 17:43:38; author: chip; state: Exp; lines: +5 -5
periodic checkin of Mon Aug 7 10:43:36 PDT 1995
=====

RCS file: /s6/cvsroot/euterpe/compass/layouts/euterpelpadtr.ly,v
Working file: compass/layouts/euterpelpadtr.ly
head: 2.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2; selected revisions: 1
description:

revision 2.2
date: 1995/08/07 17:43:40; author: chip; state: Exp; lines: +5 -5
periodic checkin of Mon Aug 7 10:43:36 PDT 1995
=====

RCS file: /s6/cvsroot/euterpe/compass/layouts/f0007.ly,v
Working file: compass/layouts/f0007.ly
head: 10.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12; selected revisions: 4
description:

revision 10.9
date: 1995/08/11 01:48:46; author: chip; state: Exp; lines: +2 -2
periodic checkin of Thu Aug 10 18:47:04 PDT 1995

revision 10.8
date: 1995/08/10 21:38:13; author: chip; state: Exp; lines: +2429 -2420
periodic checkin of Thu Aug 10 14:35:50 PDT 1995

revision 10.7
date: 1995/08/08 21:55:18; author: chip; state: Exp; lines: +1 -1
periodic checkin of Tue Aug 8 14:55:09 PDT 1995

revision 10.6
date: 1995/08/08 21:36:45; author: chip; state: Exp; lines: +2551 -21815
periodic checkin of Tue Aug 8 14:36:38 PDT 1995
=====

RCS file: /s6/cvsroot/euterpe/compass/layouts/f0007_fill_ctpg.ly,v
Working file: compass/layouts/f0007_fill_ctpg.ly
head: 19.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6; selected revisions: 3
description:

revision 19.3

date: 1995/08/11 01:49:49; author: chip; state: Exp; lines: +189689 -189880
periodic checkin of Thu Aug 10 18:47:04 PDT 1995

revision 19.2

date: 1995/08/10 21:38:52; author: chip; state: Exp; lines: +189880 -195714
periodic checkin of Thu Aug 10 14:35:50 PDT 1995

revision 19.1

date: 1995/08/08 21:56:00; author: chip; state: Exp;
periodic checkin of Tue Aug 8 14:55:09 PDT 1995

=====

RCS file: /s6/cvsroot/euterpe/compass/layouts/f0007_fill_m1.ly,v

Working file: compass/layouts/f0007_fill_m1.ly

head: 19.6

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 6; selected revisions: 3

description:

revision 19.3

date: 1995/08/11 01:52:54; author: chip; state: Exp; lines: +1 -1
periodic checkin of Thu Aug 10 18:47:04 PDT 1995

revision 19.2

date: 1995/08/10 21:41:16; author: chip; state: Exp; lines: +100898 -206776
periodic checkin of Thu Aug 10 14:35:50 PDT 1995

revision 19.1

date: 1995/08/08 21:57:48; author: chip; state: Exp;
periodic checkin of Tue Aug 8 14:55:09 PDT 1995

=====

RCS file: /s6/cvsroot/euterpe/compass/layouts/f0007_fill_m2.ly,v

Working file: compass/layouts/f0007_fill_m2.ly

head: 19.6

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 6; selected revisions: 3

description:

revision 19.3

date: 1995/08/11 01:54:19; author: chip; state: Exp; lines: +1 -1
periodic checkin of Thu Aug 10 18:47:04 PDT 1995

revision 19.2

date: 1995/08/10 21:43:04; author: chip; state: Exp; lines: +112267 -217369
periodic checkin of Thu Aug 10 14:35:50 PDT 1995

revision 19.1

date: 1995/08/08 21:59:05; author: chip; state: Exp;
periodic checkin of Tue Aug 8 14:55:09 PDT 1995

=====

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RCS file: /s6/cvsroot/euterpe/compass/layouts/f0007_fill_m3.ly,v

Working file: compass/layouts/f0007_fill_m3.ly

head: 19.6

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 6; selected revisions: 3

description:

revision 19.3

date: 1995/08/11 01:56:13; author: chip; state: Exp; lines: +1 -1

periodic checkin of Thu Aug 10 18:47:04 PDT 1995

revision 19.2

date: 1995/08/10 21:45:05; author: chip; state: Exp; lines: +111524 -218254

periodic checkin of Thu Aug 10 14:35:50 PDT 1995

revision 19.1

date: 1995/08/08 22:01:07; author: chip; state: Exp;

periodic checkin of Tue Aug 8 14:55:09 PDT 1995
=====

RCS file: /s6/cvsroot/euterpe/compass/layouts/f0007_fill_m4.ly,v

Working file: compass/layouts/f0007_fill_m4.ly

head: 19.6

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 6; selected revisions: 3

description:

revision 19.3

date: 1995/08/11 01:58:06; author: chip; state: Exp; lines: +1 -1

periodic checkin of Thu Aug 10 18:47:04 PDT 1995

revision 19.2

date: 1995/08/10 21:47:19; author: chip; state: Exp; lines: +114670 -222322

periodic checkin of Thu Aug 10 14:35:50 PDT 1995

revision 19.1

date: 1995/08/08 22:08:22; author: chip; state: Exp;

periodic checkin of Tue Aug 8 15:07:59 PDT 1995
=====

RCS file: /s6/cvsroot/euterpe/compass/layouts/f0007_fill_v12.ly,v

Working file: compass/layouts/f0007_fill_v12.ly

head: 19.6

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 6; selected revisions: 3

description:

```

revision 19.3
date: 1995/08/11 01:59:34; author: chip; state: Exp; lines: +96427 -96427
periodic checkin of Thu Aug 10 18:47:04 PDT 1995
-----
revision 19.2
date: 1995/08/10 21:49:13; author: chip; state: Exp; lines: +96427 -205561
periodic checkin of Thu Aug 10 14:35:50 PDT 1995
-----
revision 19.1
date: 1995/08/08 22:09:25; author: chip; state: Exp;
periodic checkin of Tue Aug 8 15:07:59 PDT 1995
=====

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```

RCS file: /s6/cvsroot/euterpe/compass/layouts/f0007_fill_v23.ly,v
Working file: compass/layouts/f0007_fill_v23.ly
head: 19.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;      selected revisions: 3
description:
-----

```

```

revision 19.3
date: 1995/08/11 02:01:33; author: chip; state: Exp; lines: +104084 -107577
periodic checkin of Thu Aug 10 18:47:04 PDT 1995
-----
revision 19.2
date: 1995/08/10 21:50:57; author: chip; state: Exp; lines: +107577 -214098
periodic checkin of Thu Aug 10 14:35:50 PDT 1995
-----
revision 19.1
date: 1995/08/08 22:10:30; author: chip; state: Exp;
periodic checkin of Tue Aug 8 15:07:59 PDT 1995
=====

```

```

RCS file: /s6/cvsroot/euterpe/compass/layouts/f0007_fill_v34.ly,v
Working file: compass/layouts/f0007_fill_v34.ly
head: 19.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;      selected revisions: 3
description:
-----

```

```

revision 19.3
date: 1995/08/11 02:03:45; author: chip; state: Exp; lines: +106190 -108366
periodic checkin of Thu Aug 10 18:47:04 PDT 1995
-----
revision 19.2
date: 1995/08/10 21:52:50; author: chip; state: Exp; lines: +108366 -215407
periodic checkin of Thu Aug 10 14:35:50 PDT 1995
-----
revision 19.1
date: 1995/08/08 22:11:37; author: chip; state: Exp;
periodic checkin of Tue Aug 8 15:07:59 PDT 1995

```


=====

RCS file: /s6/cvsroot/euterpe/compass/layouts/f0007_fill_v45.ly,v
Working file: compass/layouts/f0007_fill_v45.ly

head: 19.6

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 6; selected revisions: 3

description:

revision 19.3

date: 1995/08/11 02:05:53; author: chip; state: Exp; lines: +107731 -105731

periodic checkin of Thu Aug 10 18:47:04 PDT 1995

revision 19.2

date: 1995/08/10 21:54:50; author: chip; state: Exp; lines: +105731 -217300

periodic checkin of Thu Aug 10 14:35:50 PDT 1995

revision 19.1

date: 1995/08/08 22:12:53; author: chip; state: Exp;

periodic checkin of Tue Aug 8 15:07:59 PDT 1995

=====

RCS file: /s6/cvsroot/euterpe/compass/layouts/lid_euterpe_1.ly,v

Working file: compass/layouts/lid_euterpe_1.ly

head: 2.14

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 14; selected revisions: 1

description:

revision 2.5

date: 1995/08/07 17:43:53; author: chip; state: Exp; lines: +6779 -2170

periodic checkin of Mon Aug 7 10:43:36 PDT 1995

=====

RCS file: /s6/cvsroot/euterpe/compass/layouts/vlsi.cko,v

Working file: compass/layouts/vlsi.cko

head: 2.73

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 73; selected revisions: 9

description:

revision 2.37

date: 1995/08/11 02:07:24; author: chip; state: Exp; lines: +0 -10

periodic checkin of Thu Aug 10 18:47:04 PDT 1995

revision 2.36

date: 1995/08/10 23:24:41; author: chip; state: Exp; lines: +10 -0

periodic checkin of Thu Aug 10 16:24:39 PDT 1995

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revision 2.35
date: 1995/08/10 21:56:20; author: chip; state: Exp; lines: +0 -10
periodic checkin of Thu Aug 10 14:35:50 PDT 1995

revision 2.34
date: 1995/08/10 21:29:43; author: chip; state: Exp; lines: +10 -0
periodic checkin of Thu Aug 10 14:29:41 PDT 1995

revision 2.33
date: 1995/08/08 21:36:53; author: chip; state: Exp; lines: +0 -1
periodic checkin of Tue Aug 8 14:36:38 PDT 1995

revision 2.32
date: 1995/08/08 18:25:52; author: chip; state: Exp; lines: +1 -0
periodic checkin of Tue Aug 8 11:25:50 PDT 1995

revision 2.31
date: 1995/08/07 17:44:03; author: chip; state: Exp; lines: +0 -3
periodic checkin of Mon Aug 7 10:43:36 PDT 1995

revision 2.30
date: 1995/08/07 17:13:09; author: chip; state: Exp; lines: +2 -0
periodic checkin of Mon Aug 7 10:13:07 PDT 1995

revision 2.29
date: 1995/08/07 16:34:43; author: chip; state: Exp; lines: +1 -0
periodic checkin of Mon Aug 7 09:34:41 PDT 1995
=====

RCS file: /s6/cvsroot/euterpe/compass/layouts/vlsi.log,v

Working file: compass/layouts/vlsi.log

head: 2.88

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 88; selected revisions: 10

description:

revision 2.40
date: 1995/08/11 02:07:26; author: chip; state: Exp; lines: +20 -0
periodic checkin of Thu Aug 10 18:47:04 PDT 1995

revision 2.39
date: 1995/08/10 23:24:42; author: chip; state: Exp; lines: +10 -0
periodic checkin of Thu Aug 10 16:24:39 PDT 1995

revision 2.38
date: 1995/08/10 21:56:22; author: chip; state: Exp; lines: +20 -0
periodic checkin of Thu Aug 10 14:35:50 PDT 1995

revision 2.37
date: 1995/08/10 21:29:44; author: chip; state: Exp; lines: +10 -0
periodic checkin of Thu Aug 10 14:29:41 PDT 1995

revision 2.36

date: 1995/08/08 22:02:18; author: chip; state: Exp; lines: +21 -0
periodic checkin of Tue Aug 8 14:55:09 PDT 1995

revision 2.35

date: 1995/08/08 21:36:55; author: chip; state: Exp; lines: +23 -0
periodic checkin of Tue Aug 8 14:36:38 PDT 1995

revision 2.34

date: 1995/08/08 18:25:53; author: chip; state: Exp; lines: +1 -0
periodic checkin of Tue Aug 8 11:25:50 PDT 1995

revision 2.33

date: 1995/08/07 17:44:04; author: chip; state: Exp; lines: +6 -0
periodic checkin of Mon Aug 7 10:43:36 PDT 1995

revision 2.32

date: 1995/08/07 17:13:11; author: chip; state: Exp; lines: +2 -0
periodic checkin of Mon Aug 7 10:13:07 PDT 1995

revision 2.31

date: 1995/08/07 16:34:45; author: chip; state: Exp; lines: +1 -0
periodic checkin of Mon Aug 7 09:34:41 PDT 1995

=====

RCS file: /s6/cvsroot/euterpe/doc/BOM,v

Working file: doc/BOM

head: 22.5

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 70; selected revisions: 2

description:

BOM for doc

revision 22.0

date: 1995/08/10 05:28:32; author: chip; state: Exp; lines: +1 -1
Release Target: euterpe/doc

The id chip is being used by tbr.

releasing to get included in full top level release

revision 21.3

date: 1995/08/10 05:28:26; author: chip; state: Exp; lines: +6 -6
releasebom: File needs to be up-to-date to use commit -r

=====

RCS file: /s6/cvsroot/euterpe/doc/Attic/cerberus.mif,v

Working file: doc/cerberus.mif

head: 4.39

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 53; selected revisions: 1

description:

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revision 4.39

date: 1995/08/08 22:10:48; author: bobm; state: Exp; lines: +462 -66
added details to the analog test point field in octlet 31
=====

RCS file: /s6/cvsroot/euterpe/msts/DUT_boards/p620_00025_0000/ged/Makefile,v
Working file: msts/DUT_boards/p620_00025_0000/ged/Makefile
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3; selected revisions: 1
description:

revision 1.3

date: 1995/08/09 16:30:04; author: pmayer; state: Exp; lines: +7 -1
new and improved (D.Albers)
=====

RCS file:
/s6/cvsroot/euterpe/msts/DUT_boards/p620_00025_0000/ged/probes/euterpe_mms_probe
/spice.1.1,v
Working file:
msts/DUT_boards/p620_00025_0000/ged/probes/euterpe_mms_probe/spice.1.1
head: 1.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7; selected revisions: 1
description:

revision 1.2

date: 1995/08/11 04:45:03; author: pmayer; state: Exp; lines: +604 -1561
major edits to accomodate all pins to probe and tp's
=====

RCS file:
/s6/cvsroot/euterpe/msts/DUT_boards/p620_00025_0000/ged/probes/euterpe_mms_probe
/spice.1.2,v
Working file:
msts/DUT_boards/p620_00025_0000/ged/probes/euterpe_mms_probe/spice.1.2
head: 1.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6; selected revisions: 1
description:

revision 1.2

date: 1995/08/11 04:45:06; author: pmayer; state: Exp; lines: +1451 -1411
major edits to accomodate all pins to probe and tp's
=====

RCS file: /s6/cvsroot/euterpe/verify/BOM,v

Working file: verify/BOM

head: 12.34

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 404; selected revisions: 2

description:

revision 5.0

date: 1995/08/10 05:49:05; author: chip; state: Exp; lines: +1 -1

Release Target: euterpe

The id chip is being used by tbr.

full release prior to major baseplate rebuild

revision 4.204

date: 1995/08/10 05:48:58; author: chip; state: Exp; lines: +7 -25

releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verify/status,v

Working file: verify/status

head: 3.64

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 64; selected revisions: 3

description:

revision 3.51

date: 1995/08/11 02:34:24; author: dit00; state: Exp; lines: +39 -0

Update

revision 3.50

date: 1995/08/10 14:14:12; author: dit00; state: Exp; lines: +48 -2

Update

revision 3.49

date: 1995/08/09 17:24:32; author: lisar; state: Exp; lines: +107 -0

Periodic update
=====

RCS file: /s6/cvsroot/euterpe/verify/perf/dcachedirty_perf.S,v

Working file: verify/perf/dcachedirty_perf.S

head: 3.1

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 1; selected revisions: 1

description:

revision 3.1

date: 1995/08/08 22:28:14; author: claseman; state: Exp;

initial revision

```
=====
RCS file: /s6/cvsroot/euterpe/verify/perf/icache_hermes_perf.S,v
Working file: verify/perf/icache_hermes_perf.S
head: 3.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
```

```
revision 3.1
date: 1995/08/08 22:28:16; author: claseman; state: Exp;
initial revision
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/perf/icacheflush_perf.S,v
Working file: verify/perf/icacheflush_perf.S
head: 3.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
```

```
revision 3.1
date: 1995/08/08 22:28:11; author: claseman; state: Exp;
initial revision
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/toplevel/cerbparerr.S,v
Working file: verify/toplevel/cerbparerr.S
head: 40.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;      selected revisions: 1
description:
-----
```

```
revision 40.3
date: 1995/08/07 17:49:32; author: jeffm; state: Exp; lines: +2 -2
Oops - pass 2 broken.
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/toplevel/cnflct_debug.sig,v
Working file: verify/toplevel/cnflct_debug.sig
head: 33.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;      selected revisions: 1
description:
-----
```

revision 33.3
date: 1995/08/08 21:32:08; author: jeffm; state: Exp; lines: +6 -1
Added swap conflict trace signals.
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/nbleak_debug.sig,v
Working file: verify/toplevel/nbleak_debug.sig
head: 41.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2; selected revisions: 1
description:

revision 41.2
date: 1995/08/08 00:09:00; author: jeffm; state: Exp; lines: +12 -0
Added more nb internal signals.
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/template,v
Working file: verify/toplevel/template
head: 1.148
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 148; selected revisions: 3
description:

revision 1.139
date: 1995/08/11 02:36:46; author: dit00; state: Exp; lines: +5 -5
Removed set_ml3_dram_store_unique_0 from group run01

revision 1.138
date: 1995/08/10 14:17:19; author: dit00; state: Exp; lines: +8 -4
added new perf tests

revision 1.137
date: 1995/08/09 17:25:11; author: lisar; state: Exp; lines: +18 -18
LVS netlist
=====

RCS file: /s6/cvsroot/euterpe/verilog/BOM,v
Working file: verilog/BOM
head: 6.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1390; selected revisions: 8
description:
top level verilog BOM

revision 5.0
date: 1995/08/10 08:26:09; author: chip; state: Exp; lines: +1 -1
Release Target: euterpe

The id chip is being used by tbr.
top level.0 prior to major build, 2nd attempt

revision 4.24
date: 1995/08/10 08:25:58; author: chip; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r

revision 4.23
date: 1995/08/10 05:54:00; author: chip; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc
analog_euterpe.hwc

The id chip is being used by tbr.
put vddep0/1 back to 20.5

revision 4.22
date: 1995/08/10 00:01:06; author: mws; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc

cc/cc.V cc/cc_control_blob.pim:
CPlastIfetchI2 was not tau aligned and therefore could trigger cc/inprogpl to
release the same cycle as a valid dmissR12. This can result in ccstartR13 the
next cycle which is too fast for aSel to get the correct addresses loaded.
This was noticed by cachesynchnasty2_var_b_1 after the nb leak chck was added.
euterpe.V cp/cp.V cp/cphh.pim \
ce/cerberus.V ce/ce_mck.V ce/cerberus.cpiif ce/cerbttest.V ce/cerbnobreg.V:
Synchronizer for machine check edge detector.
chip_euterpe-base.pim:
Added synchronizer placements in cp area.
uu/uu.V: Comment that swapstore load pipe only def on load1st was incorrect.
uu/uustepuu.pla: Because swapstore's step0 can issue on non-eta3, address
generation must be a care. Add comments explaining barely-working
performance-hurting mess of swpBsy, swpStr, and swpLd if step0 plays on
eta2 or (worse) eta0.

revision 4.21
date: 1995/08/09 04:59:34; author: chip; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/lvs

The id chip is being used by tbr.
adding Hermes device

revision 4.20
date: 1995/08/09 04:46:20; author: chip; state: Exp; lines: +2 -2
Release Target: euterpe/verilog
Makefile

The id chip is being used by tbr.
Makefile no longer redirects outputs

revision 4.19
date: 1995/08/08 18:06:29; author: mws; state: Exp; lines: +2 -2
Release Target: euterpe/verilog/bsrc

Checkins mostly to be compatible with new more rigorous VEqn var reuse checking.
at/atpadcd.Veqn nb/nbwe.Veqn:

Was dangerously using same symbol as vector & scalar I/O (but did work OK).
hc/hc_tagmatch.V:

Delete unnecess include of hc.h, for which Makefile did not enforce dependency.
uu/sswap.tst: Specify dlva to stop align check going X.

tst/drvchk.V: Update to match new single ended CEprb[31:0].

Some ICC and CC wires were floating in mgnb testing.

tst/vervars tst/tstgen: Were referencing non-stable non-std version of perl.

revision 4.18

date: 1995/08/05 15:18:39; author: chip; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc

chip_euterpe-base.pim

The id chip is being used by tbr.

move 2 components in nb

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/BOM,v

Working file: verilog/bsrc/BOM

head: 346.6

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 1737; selected revisions: 8

description:

revision 343.0

date: 1995/08/10 08:25:25; author: chip; state: Exp; lines: +1 -1

Release Target: euterpe

The id chip is being used by tbr.

top level.0 prior to major build, 2nd attempt

revision 342.2

date: 1995/08/10 08:25:13; author: chip; state: Exp; lines: +7 -6

releasebom: File needs to be up-to-date to use commit -r

revision 342.1

date: 1995/08/10 05:53:43; author: chip; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc

analog_euterpe.hwc

The id chip is being used by tbr.

put vddep0/1 back to 20.5

revision 342.0

date: 1995/08/10 00:00:36; author: mws; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

cc/cc.V cc/cc_control_blob.pim:

CPlastIfetchI2 was not tau aligned and therefore could trigger cc/inprogpl to release the same cycle as a valid dmissR12. This can result in ccstartR13 the next cycle which is too fast for aSel to get the correct addresses loaded.

This was noticed by cachesynchnasty2_var_b_1 after the nb leak chck was added.

euterpe.V cp/cp.V cp/cphh.pim \

ce/cerberus.V ce/ce_mck.V ce/cerberus.cpf ce/cerbttest.V ce/cerbnobreg.V:

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Syncronizer for machine check edge detector.

chip_euterpe-base.pim:

Added syncronizer placements in cp area.

uu/uu.V: Comment that swapstore load pipe only def on load1st was incorrect.

uu/uustepuu.pla: Because swapstore's step0 can issue on non-eta3, address generation must be a care. Add comments explaining barely-working performance-hurting mess of swpBsy, swpStr, and swpLd if step0 plays on eta2 or (worse) eta0.

revision 341.1

date: 1995/08/10 00:00:16; author: mws; state: Exp; lines: +7 -7

releasebom: File needs to be up-to-date to use commit -r

revision 341.0

date: 1995/08/08 18:06:11; author: mws; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

Checkins mostly to be compatible with new more rigorous VEqn var reuse checking.
at/atpadcd.Veqn nb/nbwe.Veqn:

Was dangerously using same symbol as vector & scalar I/O (but did work OK).
hc/hc_tagmatch.V:

Delete unnecess include of hc.h, for which Makefile did not enforce dependency.

uu/sswap.tst: Specify dlva to stop align check going X.

tst/drvchk.V: Update to match new single ended CEprb[31:0].

Some ICC and CC wires were floating in mgnb testing.

tst/vervars tst/tstgen: Were referencing non-stable non-std version of perl.

revision 340.2

date: 1995/08/08 18:05:59; author: mws; state: Exp; lines: +6 -6

releasebom: File needs to be up-to-date to use commit -r

revision 340.1

date: 1995/08/05 15:18:24; author: chip; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc

chip_euterpe-base.pim

The id chip is being used by tbr.

move 2 components in nb
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile.share,v

Working file: verilog/bsrc/Makefile.share

head: 1.57

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 57; selected revisions: 1

description:

revision 1.57

date: 1995/08/10 07:03:24; author: chip; state: Exp; lines: +6 -1

added compent about power.tab.local ordering
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile.tst,v

Working file: verilog/bsrc/Makefile.tst

```

head: 40.104
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 104;   selected revisions: 2
description:
-----
revision 40.103
date: 1995/08/10 08:10:35; author: tbr; state: Exp; lines: +18 -64
new handling of top level power.tab. Delete obsolete junk
-----
revision 40.102
date: 1995/08/10 07:22:36; author: tbr; state: Exp; lines: +16 -13
change generation of top level power.tab to eliminate forc_(swing_)if_io
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/analog_euterpe.hwc,v
Working file: verilog/bsrc/analog_euterpe.hwc
head: 35.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;   selected revisions: 1
description:
-----

```

```

revision 35.7
date: 1995/08/10 05:53:07; author: chip; state: Exp; lines: +3 -3
put vddep0/1 back to 20.5u - tbr
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.netcap,v
Working file: verilog/bsrc/chip_euterpe-base.netcap
head: 312.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;   selected revisions: 1
description:
-----

```

```

revision 312.20
date: 1995/08/10 05:20:13; author: chip; state: Exp; lines: +33442 -33438
manual tweak to track latest logic fix
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.pim,v
Working file: verilog/bsrc/chip_euterpe-base.pim
head: 312.23
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 23;   selected revisions: 3
description:
-----

```

revision 312.22
date: 1995/08/10 05:11:21; author: chip; state: Exp; lines: +4 -0
manual tweak to track latest logic fix

revision 312.21
date: 1995/08/09 23:22:07; author: dickson; state: Exp; lines: +6 -0
added synchronizer placements in cp area

revision 312.20
date: 1995/08/05 15:17:12; author: chip; state: Exp; lines: +2 -2
move 2 components in nb

=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Attic/chip_euterpe-
base.power.tab.local,v
Working file: verilog/bsrc/chip_euterpe-base.power.tab.local
head: 340.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1; selected revisions: 1
description:

revision 340.1
date: 1995/08/10 08:11:32; author: tbr; state: Exp;
added top level power.tab.local as source file

=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.strength,v
Working file: verilog/bsrc/chip_euterpe-base.strength
head: 312.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20; selected revisions: 1
description:

revision 312.20
date: 1995/08/10 05:13:23; author: chip; state: Exp; lines: +565 -561
manual tweak to track latest logic fix

=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe.V,v
Working file: verilog/bsrc/euterpe.V
head: 6.431
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 431; selected revisions: 1
description:

revision 6.429
date: 1995/08/09 22:48:26; author: dickson; state: Exp; lines: +8 -3
synchronizer for machine check edge detector

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/BOM,v

Working file: verilog/bsrc/at/BOM

head: 93.0

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 184; selected revisions: 2

description:

releasebom adding BOM

revision 93.0

date: 1995/08/08 17:59:29; author: mws; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

Checkins mostly to be compatible with new more rigorous VEqn var reuse checking.
at/atpadcd.Veqn nb/nbwe.Veqn:

Was dangerously using same symbol as vector & scalar I/O (but did work OK).
hc/hc tagmatch.V:

Delete unnecess include of hc.h, for which Makefile did not enforce dependency.

uu/sswap.tst: Specify dlva to stop align check going X.'

tst/drvchk.V: Update to match new single ended CEprb[31:0].

Some ICC and CC wires were floating in mgnb testing.

tst/vervars tst/tstgen: Were referencing non-stable non-std version of perl.

revision 92.1

date: 1995/08/08 17:59:22; author: mws; state: Exp; lines: +2 -2

releasebom: File needs to be up-to-date to use commit -r

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/atpadcd.Veqn,v

Working file: verilog/bsrc/at/atpadcd.Veqn

head: 1.25

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 25; selected revisions: 1

description:

revision 1.25

date: 1995/08/07 20:10:56; author: woody; state: Exp; lines: +4 -4

Change internal names such that they do not match input/output names.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/BOM,v

Working file: verilog/bsrc/cc/BOM

head: 92.0

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 182; selected revisions: 2

description:

releasebom adding BOM

revision 91.0

date: 1995/08/09 23:52:00; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

cc/cc.V cc/cc_control_blob.pim:

CPlastIfetchI2 was not tau aligned and therefore could trigger cc/inprogpl to release the same cycle as a valid dmissR12. This can result in ccstartR13 the next cycle which is too fast for aSel to get the correct addresses loaded.

This was noticed by cachesynchnasty2_var_b_1 after the nb leak chck was added.

euterpe.V cp/cp.V cp/cphh.pim \

ce/cerberus.V ce/ce_mck.V ce/cerberus.cpiif ce/cerbttest.V ce/cerbnobreg.V:

Synchronizer for machine check edge detector.

chip_euterpe-base.pim:

Added synchronizer placements in cp area.

uu/uu.V: Comment that swapstore load pipe only def on load1st was incorrect.

uu/uustepuu.pla: Because swapstore's step0 can issue on non-eta3, address generation must be a care. Add comments explaining barely-working performance-hurting mess of swpBsy, swpStr, and swpLd if step0 plays on eta2 or (worse) eta0.

revision 90.1

date: 1995/08/09 23:51:52; author: mws; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/cc.V,v

Working file: verilog/bsrc/cc/cc.V

head: 1.87

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 87; selected revisions: 1

description:

revision 1.87

date: 1995/08/09 23:16:22; author: woody; state: Exp; lines: +15 -2
CPlastIfetchI2 is not tau aligned and therefore can trigger cc/inprogpl to release the same cycle as a valid dmissR12. This can result in ccstartR13 the next cycle which is too fast for aSel to get the correct addresses loaded. This was noticed by cachesynchnasty2_var_b_1.

Stretched iFillCmplt to 2 cycles and then gated it with tau such that it will not get the incorrect alignment mentioned above.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/cc_control_blob.pim,v

Working file: verilog/bsrc/cc/cc_control_blob.pim

head: 77.8

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 8; selected revisions: 1

description:

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revision 77.8

date: 1995/08/09 23:16:25; author: woody; state: Exp; lines: +9 -1
CPlastIfetchI2 is not tau aligned and therefore can trigger cc/inprogpl to
release the same cycle as a valid dmissR12. This can result in ccstartR13 the
next cycle which is too fast for aSel to get the correct addresses loaded.
This was noticed by cachesynchnasty2_var_b_1.

Stretched iFillCmplt to 2 cycles and then gated it with tau such that it will
not get the incorrect alignment mentioned above.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/ccrcv.Veqn,v

Working file: verilog/bsrc/cc/ccrcv.Veqn

head: 51.10

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 10; selected revisions: 1

description:

revision 51.10

date: 1995/08/10 21:58:50; author: mws; state: Exp; lines: +32 -10

Update comments to describe aSel-inprog spacing restriction

and the recent cc/cc.V fix:

CPlastIfetchI2 was not tau aligned and therefore could trigger cc/inprogpl to
release the same cycle as a valid dmissR12. This can result in ccstartR13 the
next cycle which is too fast for aSel to get the correct addresses loaded.

This was noticed by cachesynchnasty2_var_b_1 after the nb leak chck was added.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/BOM,v

Working file: verilog/bsrc/ce/BOM

head: 86.0

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 170; selected revisions: 2

description:

releasebom adding BOM

revision 86.0

date: 1995/08/09 23:52:39; author: mws; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

cc/cc.V cc/cc_control_blob.pim:

CPlastIfetchI2 was not tau aligned and therefore could trigger cc/inprogpl to
release the same cycle as a valid dmissR12. This can result in ccstartR13 the
next cycle which is too fast for aSel to get the correct addresses loaded.

This was noticed by cachesynchnasty2_var_b_1 after the nb leak chck was added.

euterpe.V cp/cp.V cp/cphh.pim \

ce/cerberus.V ce/ce_mck.V ce/cerberus.cpiif ce/cerbttest.V ce/cerbnobreg.V:

Synchronizer for machine check edge detector.

chip_euterpe-base.pim:

Added synchronizer placements in cp area.

uu/uu.V: Comment that swapstore load pipe only def on loadlst was incorrect.

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uu/uustepuu.pla: Because swapstore's step0 can issue on non-eta3, address generation must be a care. Add comments explaining barely-working performance-hurting mess of swpBsy, swpStr, and swpLd if step0 plays on eta2 or (worse) eta0.

revision 85.1

date: 1995/08/09 23:52:30; author: mws; state: Exp; lines: +6 -6
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/ce_mck.V,v
Working file: verilog/bsrc/ce/ce_mck.V
head: 32.14
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14; selected revisions: 1
description:

revision 32.14

date: 1995/08/09 22:47:31; author: dickson; state: Exp; lines: +8 -2
synchronizer for machine check edge detector
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cerberus.V,v
Working file: verilog/bsrc/ce/cerberus.V
head: 1.63
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 63; selected revisions: 1
description:

revision 1.58

date: 1995/08/09 22:47:33; author: dickson; state: Exp; lines: +11 -3
synchronizer for machine check edge detector
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cerberus.cpf,v
Working file: verilog/bsrc/ce/cerberus.cpf
head: 1.31
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 31; selected revisions: 1
description:

revision 1.31

date: 1995/08/09 22:48:02; author: dickson; state: Exp; lines: +3 -1
synchronizer for machine check edge detector
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cerbnobreg.V,v
Working file: verilog/bsrc/ce/cerbnobreg.V

head: 1.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7; selected revisions: 1
description:

revision 1.7
date: 1995/08/09 22:48:19; author: dickson; state: Exp; lines: +2 -2
synchronizer for machine check edge detector
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cerbtest.V,v
Working file: verilog/bsrc/ce/cerbtest.V
head: 1.46
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 46; selected revisions: 1
description:

revision 1.44
date: 1995/08/09 22:48:22; author: dickson; state: Exp; lines: +6 -2
synchronizer for machine check edge detector
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/BOM,v
Working file: verilog/bsrc/cp/BOM
head: 60.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 119; selected revisions: 2
description:
releasebom adding BOM

revision 60.0
date: 1995/08/09 23:53:29; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

cc/cc.V cc/cc_control_blob.pim:

 CPlastIfetchI2 was not tau aligned and therefore could trigger cc/inprogpl to
 release the same cycle as a valid dmissR12. This can result in ccstartR13 the
 next cycle which is too fast for aSel to get the correct addresses loaded.

 This was noticed by cachesynchnasty2_var_b_1 after the nb leak chck was added.
euterpe.V cp/cp.V cp/cphh.pim \

ce/cerberus.V ce/ce_mck.V ce/cerberus.cpfif ce/cerbtest.V ce/cerbnobreg.V:

 Synchronizer for machine check edge detector.

chip_euterpe-base.pim:

 Added synchronizer placements in cp area.

uu/uu.V: Comment that swapstore load pipe only def on load1st was incorrect.

uu/uustepuu.pla: Because swapstore's step0 can issue on non-eta3, address
 generation must be a care. Add comments explaining barely-working
 performance-hurting mess of swpBsy, swpStr, and swpLd if step0 plays on

eta2 or (worse) eta0.

revision 59.1

date: 1995/08/09 23:53:22; author: mws; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/cp.V,v

Working file: verilog/bsrc/cp/cp.V

head: 1.39

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 39; selected revisions: 1

description:

revision 1.36

date: 1995/08/09 22:47:52; author: dickson; state: Exp; lines: +11 -2
synchronizer for machine check edge detector
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/cphh.pim,v

Working file: verilog/bsrc/cp/cphh.pim

head: 47.4

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 4; selected revisions: 1

description:

revision 47.4

date: 1995/08/09 22:47:56; author: dickson; state: Exp; lines: +6 -0
synchronizer for machine check edge detector
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/BOM,v

Working file: verilog/bsrc/hc/BOM

head: 125.0

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 250; selected revisions: 2

description:

releasebom adding BOM

revision 124.0

date: 1995/08/08 18:02:05; author: mws; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

Checkins mostly to be compatible with new more rigorous VEqn var reuse checking.
at/atpadcd.Veqn nb/nbwe.Veqn:

Was dangerously using same symbol as vector & scalar I/O (but did work OK).

hc/hc_tagmatch.V:

Delete unnecess include of hc.h, for which Makefile did not enforce dependency.

uu/sswap.tst: Specify dlva to stop align check going X.
tst/drvchk.V: Update to match new single ended CEprb[31:0].
Some ICC and CC wires were floating in mgnb testing.
tst/vervars tst/tstgen: Were referencing non-stable non-std version of perl.

revision 123.1

date: 1995/08/08 18:01:57; author: mws; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc_tagmatch.V,v

Working file: verilog/bsrc/hc/hc_tagmatch.V

head: 3.5

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 5; selected revisions: 1

description:

revision 3.5

date: 1995/08/07 22:20:35; author: mws; state: Exp; lines: +1 -2

Delete unnecess include of hc.h, for which Makefile did not enforce dependncy.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/io/netcap_getSpiceNets.txt,v

Working file: verilog/bsrc/io/netcap_getSpiceNets.txt

head: 46.2

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 2; selected revisions: 1

description:

revision 46.1

date: 1995/08/10 19:50:37; author: woody; state: Exp;

Check in the info used by bill to spice the io clock paths.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/nb/BOM,v

Working file: verilog/bsrc/nb/BOM

head: 130.0

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 261; selected revisions: 2

description:

releasebom adding BOM

revision 130.0

date: 1995/08/08 18:03:32; author: mws; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

Checkins mostly to be compatible with new more rigorous VEqn var reuse checking.
at/atpadcd.Veqn nb/nbwe.Veqn:

Was dangerously using same symbol as vector & scalar I/O (but did work OK).
hc/hc_tagmatch.V:

Delete unnecess include of hc.h, for which Makefile did not enforce dependency.
uu/sswap.tst: Specify dlva to stop align check going X.

tst/drvchk.V: Update to match new single ended CEprb[31:0].

Some ICC and CC wires were floating in mgnb testing.

tst/vervars tst/tstgen: Were referencing non-stable non-std version of perl.

revision 129.1

date: 1995/08/08 18:03:25; author: mws; state: Exp; lines: +2 -2

releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/nb/nbwe.Veqn,v

Working file: verilog/bsrc/nb/nbwe.Veqn

head: 15.7

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 7; selected revisions: 1

description:

revision 15.7

date: 1995/08/07 20:21:25; author: woody; state: Exp; lines: +6 -6

Change internal names such that they do not match input/output names per new
Veqn check
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/tst/BOM,v

Working file: verilog/bsrc/tst/BOM

head: 112.0

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 234; selected revisions: 2

description:

releasebom adding BOM

revision 111.0

date: 1995/08/08 18:04:25; author: mws; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

Checkins mostly to be compatible with new more rigorous VEqn var reuse checking.
at/atpadcd.Veqn nb/nbwe.Veqn:

Was dangerously using same symbol as vector & scalar I/O (but did work OK).
hc/hc_tagmatch.V:

Delete unnecess include of hc.h, for which Makefile did not enforce dependency.
uu/sswap.tst: Specify dlva to stop align check going X.

tst/drvchk.V: Update to match new single ended CEprb[31:0].

Some ICC and CC wires were floating in mgnb testing.

tst/vervars tst/tstgen: Were referencing non-stable non-std version of perl.

revision 110.1

date: 1995/08/08 18:04:18; author: mws; state: Exp; lines: +4 -4

releasebom: File needs to be up-to-date to use commit -r

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/tst/drvchk.V,v
Working file: verilog/bsrc/tst/drvchk.V

head: 1.85

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 85; selected revisions: 1

description:

revision 1.84

date: 1995/08/07 23:28:52; author: mws; state: Exp; lines: +7 -2

tst/drvchk.V: Update to match new single ended CEprb[31:0].

Some ICC and CC wires were floating in mgnb testing.

tst/vervars tst/tstgen: Were referencing non-stable non-std version of perl.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/tst/tstgen,v

Working file: verilog/bsrc/tst/tstgen

head: 3.8

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 8; selected revisions: 1

description:

revision 3.8

date: 1995/08/07 23:28:54; author: mws; state: Exp; lines: +2 -1

tst/drvchk.V: Update to match new single ended CEprb[31:0].

Some ICC and CC wires were floating in mgnb testing.

tst/vervars tst/tstgen: Were referencing non-stable non-std version of perl.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/tst/vervars,v

Working file: verilog/bsrc/tst/vervars

head: 3.2

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 2; selected revisions: 1

description:

revision 3.2

date: 1995/08/07 23:28:55; author: mws; state: Exp; lines: +1 -1

tst/drvchk.V: Update to match new single ended CEprb[31:0].

Some ICC and CC wires were floating in mgnb testing.

tst/vervars tst/tstgen: Were referencing non-stable non-std version of perl.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/BOM,v

Working file: verilog/bsrc/uu/BOM

head: 218.1

branch:

Exhibit 4C

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```

locks: strict
access list:
keyword substitution: kv
total revisions: 480;   selected revisions: 4
description:
-----
revision 217.0
date: 1995/08/09 23:58:58; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

cc/cc.V cc/cc_control_blob.pim:
  CPlastiFetchI2 was not tau aligned and therefore could trigger cc/inprogpl to
  release the same cycle as a valid dmissR12. This can result in ccstartR13 the
  next cycle which is too fast for aSel to get the correct addresses loaded.
  This was noticed by cachesynchnasty2_var_b_1 after the nb leak chck was added.
euterpe.V cp/cp.V cp/cphh.pim \
ce/cerberus.V ce/ce_mck.V ce/cerberus.cpfif ce/cerbttest.V ce/cerbnobreg.V:
  Synchronizer for machine check edge detector.
chip_euterpe-base.pim:
  Added synchronizer placements in cp area.
uu/uu.V: Comment that swapstore load pipe only def on loadlst was incorrect.
uu/uustepuu.pla: Because swapstore's step0 can issue on non-eta3, address
  generation must be a care. Add comments explaining barely-working
  performance-hurting mess of swpBsy, swpStr, and swpLd if step0 plays on
  eta2 or (worse) eta0.
-----
revision 216.1
date: 1995/08/09 23:58:49; author: mws; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
-----
revision 216.0
date: 1995/08/08 18:04:55; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

Checkins mostly to be compatible with new more rigorous VEqn var reuse checking.
at/atpadcd.Veqn nb/nbwe.Veqn:
  Was dangerously using same symbol as vector & scalar I/O (but did work OK).
hc/hc_tagmatch.V:
  Delete unnecess include of hc.h, for which Makefile did not enforce dependncy.
uu/sswap.tst: Specify dlva to stop align check going X.
tst/drvchk.V: Update to match new single ended CEprb[31:0].
  Some ICC and CC wires were floating in mgnb testing.
tst/vervars tst/tstgen: Were referencing non-stable non-std version of perl.
-----
revision 215.1
date: 1995/08/08 18:04:47; author: mws; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/sswap.tst,v
Working file: verilog/bsrc/uu/sswap.tst
head: 125.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;   selected revisions: 1

```

description:

revision 125.7

date: 1995/08/07 23:28:18; author: mws; state: Exp; lines: +3 -3
Specify dlva to stop align check going X.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu.V,v

Working file: verilog/bsrc/uu/uu.V

head: 1.202

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 202; selected revisions: 1

description:

issue unit

revision 1.200

date: 1995/08/09 23:50:18; author: mws; state: Exp; lines: +3 -3

uu/uu.V: Comment that swapstore load pipe only def on load1st was incorrect.

uu/uustepuu.pla: Because swapstore's step0 can issue on non-eta3, address generation must be a care. Add comments explaining barely-working performance-hurting mess of swpBsy, swpStr, and swpLd if step0 plays on eta2 or (worse) eta0.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uustepuu.pla,v

Working file: verilog/bsrc/uu/uustepuu.pla

head: 84.16

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 16; selected revisions: 1

description:

revision 84.16

date: 1995/08/09 23:50:23; author: mws; state: Exp; lines: +16 -7

uu/uu.V: Comment that swapstore load pipe only def on load1st was incorrect.

uu/uustepuu.pla: Because swapstore's step0 can issue on non-eta3, address generation must be a care. Add comments explaining barely-working performance-hurting mess of swpBsy, swpStr, and swpLd if step0 plays on eta2 or (worse) eta0.
=====

RCS file: /s6/cvsroot/euterpe/verilog/lvs/BOM,v

Working file: verilog/lvs/BOM

head: 3.0

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 5; selected revisions: 2

description:

revision 3.0

date: 1995/08/09 04:59:19; author: chip; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/lvs

The id chip is being used by tbr.
adding Hermes device

revision 2.1

date: 1995/08/09 04:59:12; author: chip; state: Exp; lines: +3 -1
releasebom: File needs to be up-to-date to use commit -r
=====